

Notice of References Cited	Application/Control No. 10/661,248		Applicant(s)/Patent Under Reexamination VARNERIN ET AL.	
	Examiner Eric B. Chen		Art Unit 1765	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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	B	US-5,904,563	05-1999	Yu, Chen-Hua Douglas	438/672
	C	US-5,926,720	07-1999	Zhao et al.	438/401
	D	US-6,136,662	10-2000	Allman et al.	438/401
	E	US-5,783,490	07-1998	Tseng, Horng-Huei	438/692
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	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Wolf et al., Silicon Processing for the VLSI Era, 1986, Lattice Press, Vol. 1, pp. 176-77, 191, 432, 438-39, 441, 531, 534.
	V	Wolf, Silicon Processing for the VLSI Era, 2002, Lattice Press, Vol. 4, pp. 673, 712, 716, 718.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.